IN THE SPECIFICATION:

Please amend the specification as follows:

Please amend paragraph [004] on pages 2 and 3 as follows:

[004] One use of the overflow detector of the present invention is in a FIR (~~fast~~ finite impulse response) filter using a fast floating point multiply-accumulate (FMAC) unit, which multiplies input operands and accumulates them with the previous multiplication result. An FMAC unit is depicted in Figure 1. In this implementation, the addition 46 is performed in carry-save format so that it can be performed quickly. The adder receives input operands 43 and 44 and transmits results in carry-save format. It is necessary to predict whether the result of the addition has overflowed so that compensation with a right shifter 47 can be performed before the mantissa sum is transmitted to an earlier stage of the multiplier-accumulator circuit. Since the result is in carry-save format, this is not trivial. It is especially difficult because carry-save format addition does not follow the rules of "normal" addition.